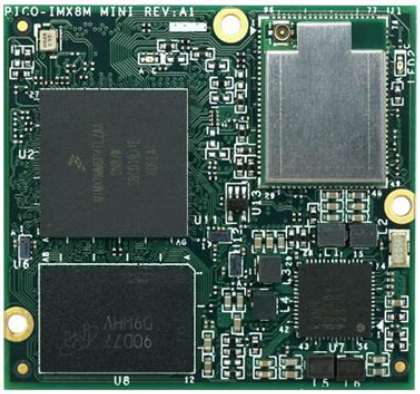


PICO-IMX8M-Mini SYSTEM ON MODULE PRODUCT MANUAL

(WITH NXP i.MX8M Mini SoC)

VER. 1.02

January 31, 2020

REVISION HISTORY

Revision	Date	Originator	Notes
0.1	November 6, 2018	TechNexion	Preliminary
1.00	March 14, 2019	TechNexion	General Public Release
1.01	October 22, 2019	TechNexion	Clarification on pinout for UART and PCIe signals
1.02	January 31, 2020	TechNexion	Correction of pin E1_17 and E1_36 in table and subsection of PMIC Added connector name labels in figure 5.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

1. Introduction

1.1. General Introduction

The PICO-IMX8M-Mini is a high performance highly integrated PICO Compute Module designed around the NXP i.MX8M Mini Quad core ARM Cortex-A53 + Cortex-M4 applications processor. The PICO-IMX8M-Mini provides an ideal building block that easily integrates with a wide range of target markets requiring compact, cost effective with low power consumption.

The modular approach offered by the PICO Compute Module gives your project scalability, fast time to market and upgradability while reducing engineering risk and maintain a competitive total cost of ownership.

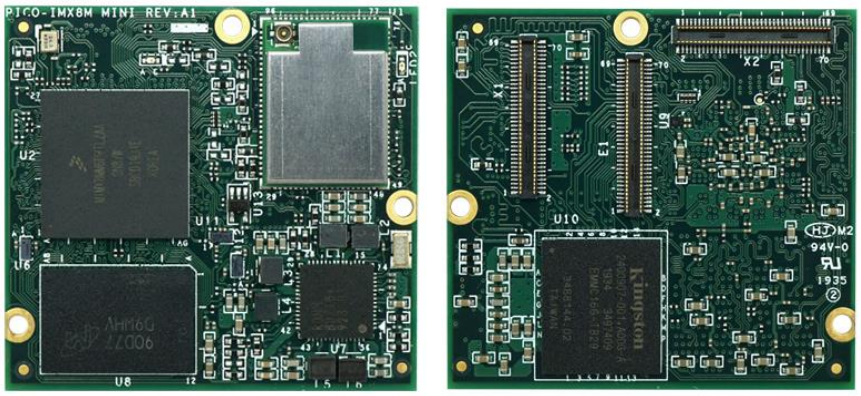
2. PICO-IMX8M-Mini Product Overview

The PICO-IMX8M-Mini is a high performance, versatile System-on-Module in PICO form factor optimized for audio, voice, video streaming applications.

2.1. PICO-IMX8M-Mini System-on-Module Overview

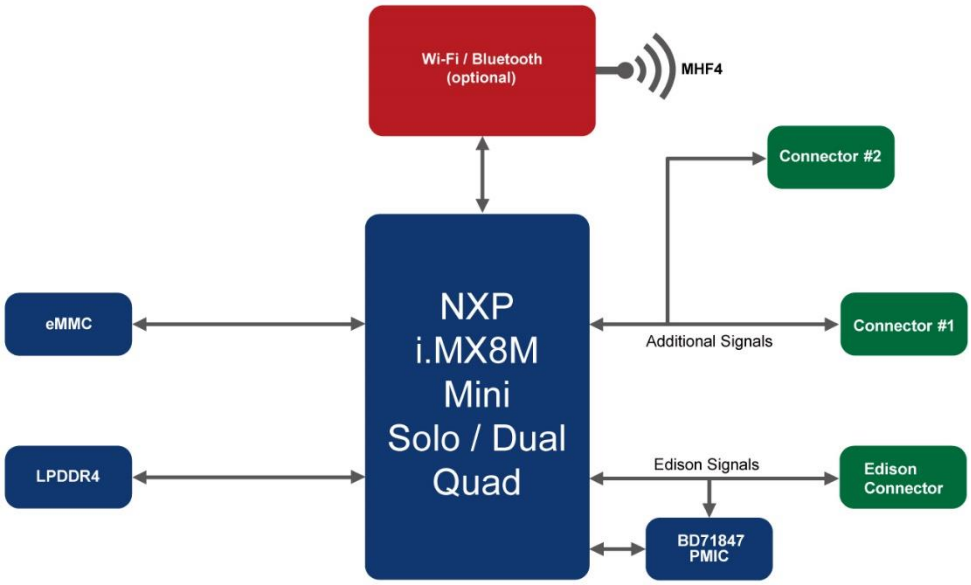
The PICO-IMX8M-Mini System-on-Module has 3 Hirose high-speed 70 pin board-to-board connectors and integrates the NXP i.MX8M Mini, Memory, eMMC, Power Management IC (PMIC) and Wi-Fi / Bluetooth features.

Figure 1 – PICO-IMX8M-Mini System-on-Module



2.2. Block Diagram

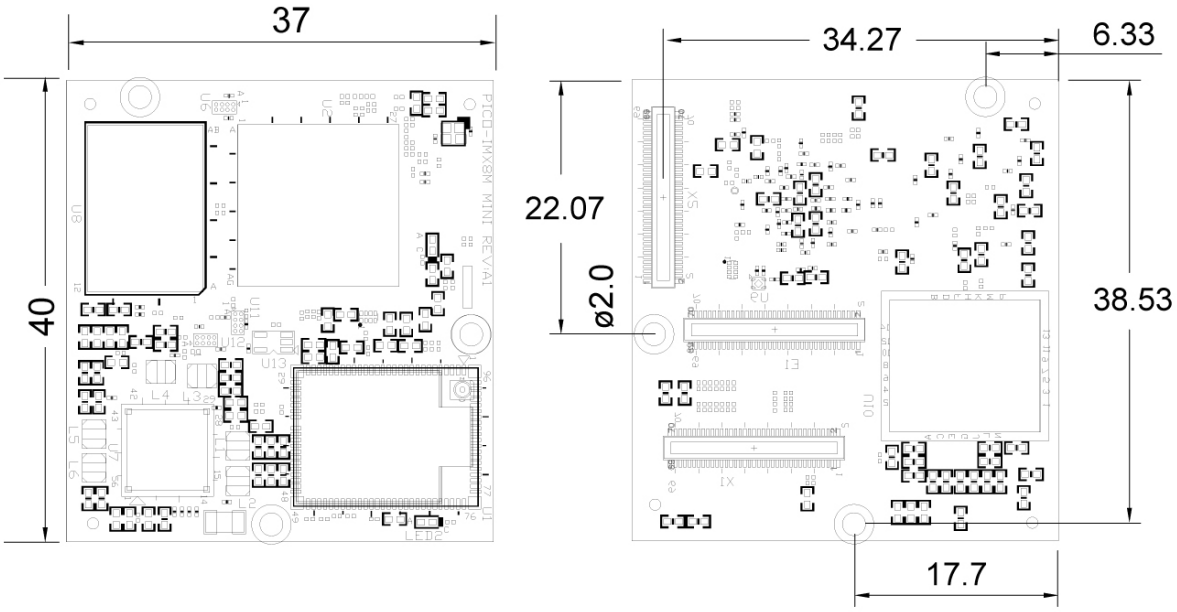
Figure 2 – PICO-IMX8-Mini System-on-Module Block Diagram Overview



2.3. Dimensional Drawing

The PICO-IMX8-Mini System-on-Module is an ultra-compact module in PICO form factor.

Figure 3 – PICO-IMX8-Mini System-on-Module Dimensions



2.4. Component Location

Figure 4 – PICO-IMX8M-Mini Top View

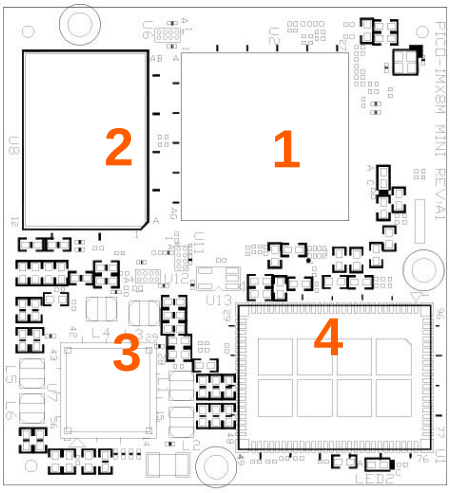
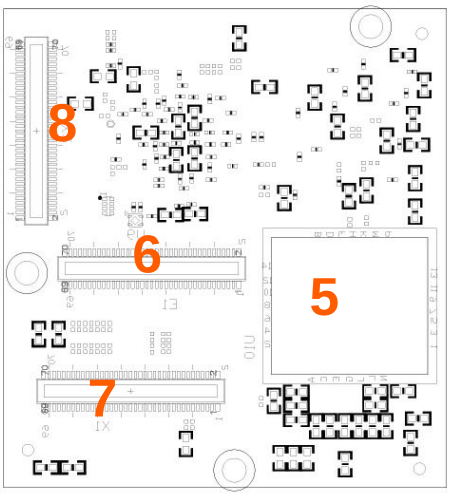


Figure 5 – PICO-IMX8M-Mini Bottom View



No.	Description	No.	Description
1	NXP i.MX8M Mini Processor	5	eMMC Storage IC
2	Memory IC	6	Connector E1
3	ROHM BD71847 PMIC	7	Connector X1
4	Wi-Fi/Bluetooth Module (optional)	8	Connector X2

3. Core Components

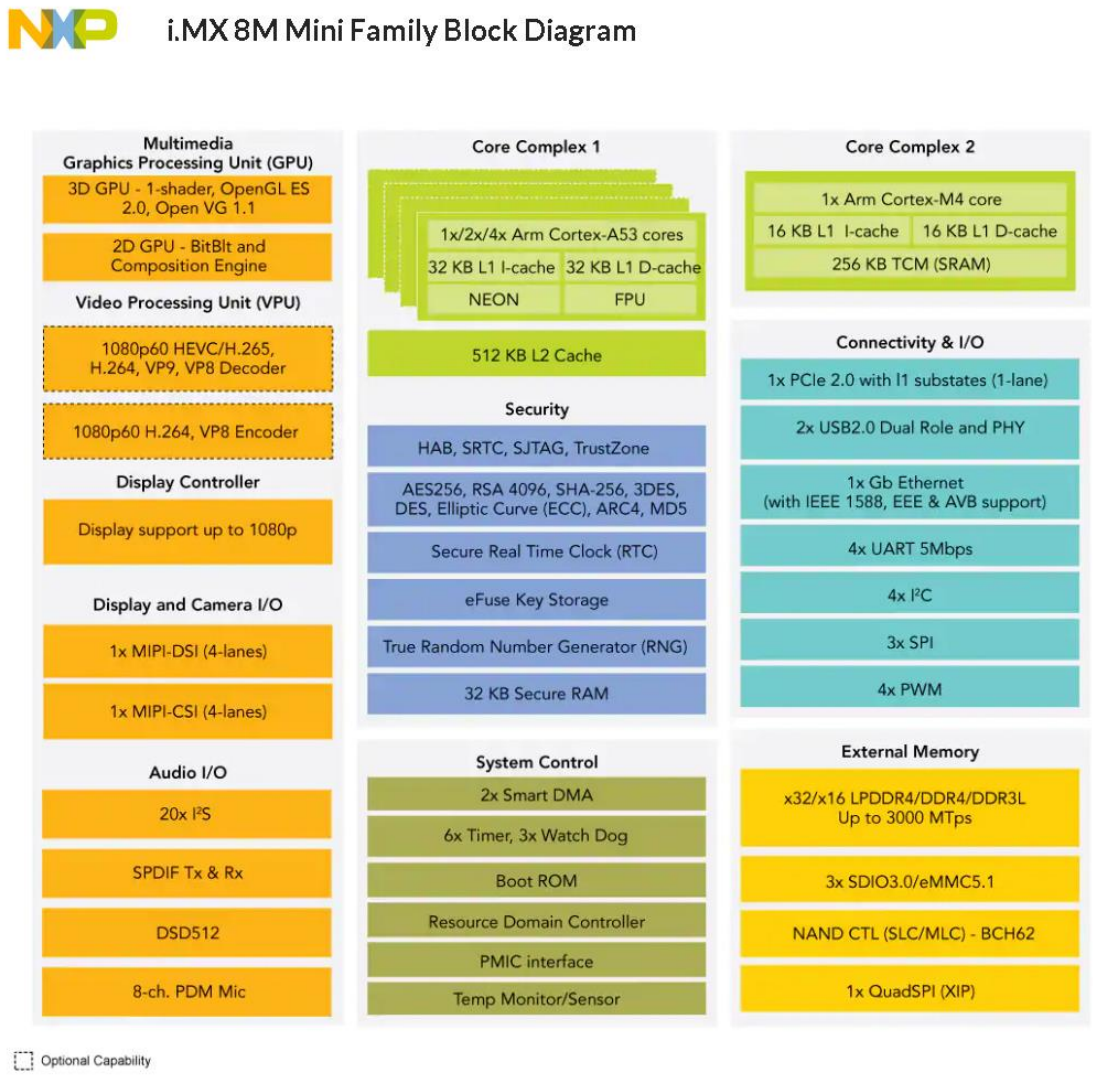
3.1. NXP i.MX8M Mini ARM Cortex-A53 + Cortex-M4 audio, Voice, Video Processor

The i.MX 8M Mini is NXP's first embedded multicore applications processor built using advanced 14LPC FinFET process technology, providing more speed and improved power efficiency. With commercial and industrial level qualification and backed by NXP's product longevity program, the i.MX 8M Mini family may be used in any general purpose industrial and IoT application.

Features:

- Multicore Processing
  - 4x Cortex-A53 core platforms up to 1.8GHz per core
  - 32KB L1-I Cache/ 32 kB L1-D Cache
  - 512 kB L2 Cache
  - 1x Arm Cortex-M4 core up to 400MHz
  - 16 kB L1-I Cache/ 16 kB L2-D Cache
- GPU
  - 3D GPU (1x shader, OpenGL ES 2.0)
  - 2D GPU
- Display Interface
  - 1x MIPI DSI (4-lane) with PHY
- Video Playback
  - 1080p60 VP9 Profile 0, 2 (10-bit) decoder, HEVC/H.265 decoder, AVC/H.264 Baseline, Main, High decoder, VP8 decoder
  - 1080p60 AVC/H.264 encoder, VP8 encoder
- Audio
  - 5x SAI (12Tx + 16Rx external I2S lanes), 8ch PDM input
- Camera Interface
  - 1x MIPI CSI (4-lane) with PHY
- USB
  - 2x USB 2.0 OTG controllers with integrated PHY
- PCIe
  - 1x PCIe 2.0 (1-lane) with L1 low power sub states
- Ethernet
  - 1x Gigabit Ethernet (MAC) with AVB and IEEE 1588, Energy Efficient Ethernet (EEE) for low power
- Operating Systems
  - Linux, Android, FreeRTOS
- Temperature
  - Consumer (0°C to 95°C Tj)
  - Industrial (-40°C to 105°C Tj)
- Package
  - FCBGA, 14x14 0.5mm pitch

Figure 6 – NXP i.MX8M-Mini Processor Blocks



3.2. Power Management IC (ROHM BD71847)

The PICO-IMX8M-Mini has an on onboard ROHM BD71847 power management integrated circuit (PMIC) that features a configurable architecture supporting the numerous outputs with various current ratings as well as programmable voltage and sequencing required by the components on the PICO-IMX8M-Mini module.

Table 1 – PMIC Signal Description

CPU BALL	CPU PAD NAME	Pinmux (mode)	PMIC Signal	V	I/O	Description
F9	I2C1_SDA	I2C1_SDA	SDA	3V3	I/O	I2C bus data line
E9	I2C1_SCL	I2C1_SCL	SCL	3V3	I	I2C bus clock line
A25	ONOFF	ONOFF	PWRON_B	3V3	I	PMIC Power ON/OFF Input from processor
B24	POR_B	POR_B	POR_B	3V3	O	PMIC Reset Signal
A24	PMIC_ON_REQ	PMIC_ON_REQ	PMIC_ON_REQ	3V3	I	PMIC Power on request Input from processor
E24	PMIC_STBY_REQ	PMIC_STBY_REQ	PMIC_STBY_REQ	3V3	I	PMIC Power standby request input from processor
AF13	GPIO1_IO03	GPIO1_IO03	IRQ_B	3V3	O	PMIC Interrupt Signal
F24	RTC_RESET_B	RTC_RESET_B	RTC_RESET_B	3V3	O	PMIC RTC Reset Signal
A26	RTC_XTALI	RTC_XTALI	C32K_OUT	3V3	O	32.768 KHz Clock

3.2.1. ROHM BD71847 Reset Signal

To perform a hard-reset of the PICO-IMX8M-Mini a software reset signal can be implemented.

Table 2 – PMIC Reset Signal Description

CPU BALL	CPU PAD NAME	Pinmux (mode)	Signal	V	I/O	Description
AG13	GPIO1_IO02	WDOG1_B	WDOG_B	3V3	I	Connected to the WDOG_B signal of PMIC

3.2.2. Hard-Reset Signal

To perform a hard-reset of the PICO-IMX8M-Mini an external circuit (for example a button or external watchdog IC) can be integrated on the carrier board.

Table 3 – PMIC Reset Signal Description

Connector	Signal	V	I/O	Description
E1_36	RESET IN	1V8	I	Connected to Reset Power Signal

The Reset signal will be triggered when pulled to ground.

3.3. Memory

The PICO-IMX8M-Mini integrates Low Power Double Data Rate IV (LPDDR4) Synchronous DRAM is connected over a 32-Bit dual channel configuration. (16 bit per channel).

The following memory chip manufacturers have been validated and tested on the PICO-IMX8M-Mini Compute Module:

- SKHynix
- Kingston
- Micron
- Samsung
- ISSI

3.4. eMMC Storage

The PICO-IMX8M-Mini can be ordered with onboard eMMC storage in different configurations and capacity. The onboard eMMC device is connected on the USDHC3 pins of the i.MX8M Mini processor in an 8-bit width configuration.

The following eMMC chip manufacturers have been validated and tested on the PICO-IMX8M-Mini System-on-Module:

- Kingston eMMC
- Micron eMMC
- Sandisk iNAND

Table 4 – eMMC Signal Description

CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
M26	NAND_DATA04	USDHC3_DATA0	1V8	I/O	MMC/SDIO Data bit 0
L26	NAND_DATA05	USDHC3_DATA1	1V8	I/O	MMC/SDIO Data bit 1
K26	NAND_DATA06	USDHC3_DATA2	1V8	I/O	MMC/SDIO Data bit 2
N26	NAND_DATA07	USDHC3_DATA3	1V8	I/O	MMC/SDIO Data bit 3
N27	NAND_RE_B	USDHC3_DATA4	1V8	I/O	MMC/SDIO Data bit 4
M27	NAND_CE2_B	USDHC3_DATA5	1V8	I/O	MMC/SDIO Data bit 5
L27	NAND_CE3_B	USDHC3_DATA6	1V8	I/O	MMC/SDIO Data bit 6
K27	NAND_CLE	USDHC3_DATA7	1V8	I/O	MMC/SDIO Data bit 7
R27	NAND_WP_B	USDHC3_CMD	1V8	I/O	MMC/SDIO Command
R26	NAND_WE_B	USDHC3_CLK	1V8	O	MMC/SDIO Clock
P27	NAND_CE1_B	USDHC3_STROBE	1V8	O	This signal is generated by the device and used for output in HS400 Mode

3.5. Wi-Fi/Bluetooth

The PICO-IMX8M-Mini has an optional pre-certified high-performance TechNexion PIXI-9377 dual band 2.4/5Ghz Wi-Fi / Bluetooth 5 Qualcomm Atheros QCA9377 based module on board.

The PIXI-9377 Wi-Fi / Bluetooth module is designed to operate with a single antenna for Wi-Fi and Bluetooth by using the MHF4 connector.

Key Features of the PIXI-9377 are:

- IEEE 802.11 ac/a/b/g/n 2.4 / 5Ghz
- Bluetooth 5
- MHF4 antenna connector
- Linux and Android drivers
- Wi-Fi / BT module board certifications with multiple antennas:
    - FCC (USA)
    - IC (Canada
    - ETSI (Europe)
    - Giteki / Telec (Japan)
    - RCM / C-tick (Australia / New Zealand).
- Industrial operation temperature range: -40°C to +85°C

The following pre-certified matching antennas are available with our distributors.

Partnumber	Description
ANTP180A138045D2450MHF4	4.5dBi dipole antenna
ANTP180A207070D2450MHF4	7dBi dipole antenna
ANTP150P232525D2450MHF4	2.5dBi PCB patch antenna

Figure 7 – PICO-IMX8M-Mini Wi-Fi Module and Antenna Connector Location

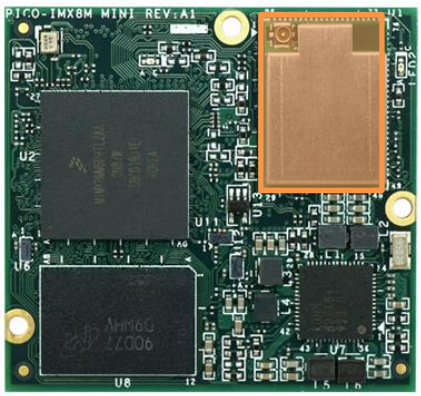


Table 5 – Wi-Fi Signal Description

i.MX8M BALL	PAD NAME	Signal	I/O	Description
Y27	SD1_DATA0	USDHC1_DATA0	I/O	MMC/SDIO Data bit 0
Y26	SD1_DATA1	USDHC1_DATA1	I/O	MMC/SDIO Data bit 1
T27	SD1_DATA2	USDHC1_DATA2	I/O	MMC/SDIO Data bit 2
T26	SD1_DATA3	USDHC1_DATA3	I/O	MMC/SDIO Data bit 3
V27	SD1_CMD	USDHC1_CMD	I/O	MMC/SDIO Command
V26	SD1_CLK	USDHC1_CLK	O	MMC/SDIO Clock
AC19	SAI2_RXFS	GPIO4_IO21 WL_HOST_WAKE	O	Host wake up. Signal from the module to the host indicating that the module requires Attention. • Asserted: Host device must wake-up or remain awake. • Deserted: Host device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.
AC10	GPIO1_IO11	GPIO1_IO11 WL_REG_ON	O	Wi-Fi device wake-up: Signal from the host to the module indicating that the host requires attention. • Asserted: Wi-Fi device must wake-up or remain awake. • Deserted: Wi-Fi device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.

Table 6 – Bluetooth Signal Description

i.MX8M BALL	PAD NAME	Signal	I/O	Description
F13	UART1_TXD	UART1_TXD	O	Bluetooth UART Serial Input. Serial data input for the HCI UART Interface
E14	UART1_RXD	UART1_RXD	I	Bluetooth UART Serial Output. Serial data output for the HCI UART Interface.
E18	UART3_RXD	UART1_CTS	I/O	Bluetooth UART Clear to Send. Active-low clear-to-send signal for the HCI UART interface.
D18	UART3_TXD	UART1_RTS	I/O	Bluetooth UART Request to Send. Active-low request-to-send signal for the HCI UART interface.
AG15	SAI1_RXD0	SAI1_RXD0	I	Integrated Interchip Sound (I^2S) channel receive data line
AG20	SAI1_TXD0	SAI1_TXD0	O	Integrated Interchip Sound (I^2S) channel transmit data line
AC18	SAI1_TXC	SAI1_TXC	O	Integrated Interchip Sound (I^2S) channel word clock signal
AB19	SAI1_TXFS	SAI1_TXFS	O	Integrated Interchip Sound (I^2S) channel frame synchronization signal
AB22	SAI2_RXC	GPIO4_IO22 BT_HOST_WAKE	I	Host UART wake up. Signal from the module to the host indicating that the module requires Attention. • Asserted: Host device must wake-up or remain awake. • Deserted: Host device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.
AB10	GPIO1_IO12	GPIO1_IO12 BT_DEV_WAKE	O	Bluetooth device wake-up: Signal from the host to the module indicating that the host requires attention. • Asserted: Bluetooth device must wake-up or remain awake. • Deserted: Bluetooth device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.

4. PICO Compute Module Pin Assignment

The PICO-IMX8M-Mini has three 70-pin Hirose board-to-board connectors.

Figure 8 – PICO-IMX8M-Mini Board-to-Board Connectors

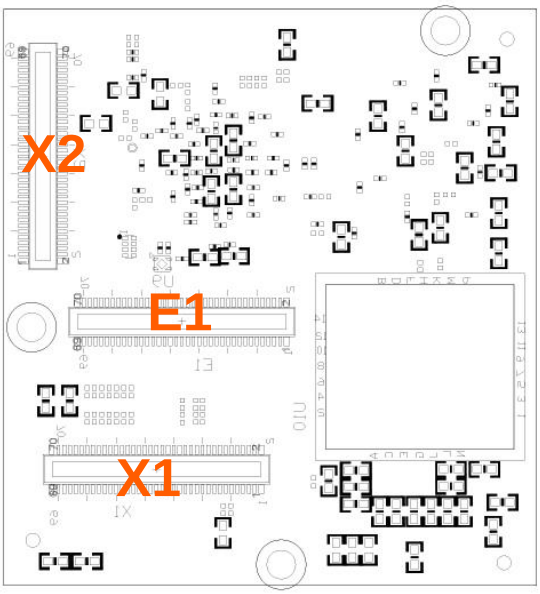


Table 7 – PICO Compute Module Pin Assignment

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
E1_1		GND	GND		P	Ground
E1_2			VSYS		P	System input power (4.2 to 5.25V)
E1_3	D22	USB1_ID	USB1_ID	3V3	I	USB OTG ID Pin
E1_4			VSYS		P	System input power (4.2 to 5.25V)
E1_5		GND	GND		P	Ground
E1_6			VSYS		P	System input power (4.2 to 5.25V)
E1_7			NC			Not Connected
E1_8		VDD_3V3	VDD_3V3	3V3	P	System 3.3V Output
E1_9		GND	GND		P	Ground
E1_10		VDD_3V3	VDD_3V3	3V3	P	System 3.3V Output
E1_11		GND	GND		P	Ground
E1_12		VDD_1V8	VDD_1V8	1V8	P	System 1.8V Output (same as E1 connector I/O voltage levels)
E1_13		GND	GND		P	Ground
E1_14			VSYS		P	System input power (4.2 to 5.25V)
E1_15		GND	GND		P	Ground
E1_16	B22	USB1_DP	USB1_DP	3V3	I/O	Universal Serial Bus differential pair positive signal
E1_17	A25	ONOFF	ONOFF	3V3	I	Power ON button input signal

						(Recommended to keep floating)
E1_18	A22	USB1_DN	USB1_DN	3V3	I/O	Universal Serial Bus differential pair negative signal
E1_19	AG7	SAI3_RXC	GPIO4_IO29	1V8	I	Over current detect input pin to monitor USB power over current
E1_20	F22	USB1_VBUS	USB1_VBUS	5V	I/O	Universal Serial Bus power
E1_21	AF10	GPIO1_IO09	USDHC3_RESET_B	1V8	O	Universal Serial Bus power enable
E1_22	F15	UART2_RXD	UART2_RXD	1V8	I	Universal Asynchronous Receive Transmit receive data signal
E1_23			NC			Not Connected
E1_24	N24	NAND_CE0_B	GPIO3_IO01	1V8	I/O	General Purpose Input Output
E1_25	N22	NAND_ALE	GPIO3_IO00	1V8	I/O	General Purpose Input Output
E1_26	P26	NAND_READY_B	GPIO3_IO16	1V8	I/O	General Purpose Input Output
E1_27	E15	UART2_TXD	UART2_TXD	1V8	O	Universal Asynchronous Receive Transmit transmit data signal
E1_28	P23	NAND_DATA00	GPIO3_IO06	1V8	I/O	General Purpose Input Output
E1_29	AG12	GPIO1_IO04	GPIO1_IO04	3V3	O	SD Card voltage select
E1_30	K24	NAND_DATA01	GPIO3_IO07	1V8	I/O	General Purpose Input Output
E1_31			NC			Not Connected
E1_32	K23	NAND_DATA02	GPIO3_IO08	1V8	I/O	General Purpose Input Output
E1_33	AG9	SPDIF_RX	PWM2_OUT	1V8	O	General Purpose Input Output with PWM control
E1_34	N23	NAND_DATA03	GPIO3_IO09	1V8	I/O	General Purpose Input Output
E1_35	AF8	SPDIF_EXT_CLK	PWM1_OUT	1V8	O	General Purpose Input Output with PWM control
E1_36			RESET IN	1V8	I	Reset power signal for PMIC
E1_37	AF9	SPDIF_TX	PWM3_OUT	1V8	I/O	General Purpose Input Output with PWM control
E1_38			NC			Not Connected
E1_39	AD6	SAI3_MCLK	PWM4_OUT	1V8	O	General Purpose Input Output with PWM control
E1_40			NC			Not Connected
E1_41	D10	I2C2_SCL	I2C2_SCL	1V8	O	I2C bus clock line
E1_42	AG8	SAI3_RXFS	GPIO4_IO28	1V8	I/O	General Purpose Input Output
E1_43	D9	I2C2_SDA	I2C2_SDA	1V8	I/O	I2C bus data line

E1_44	D13	I2C4_SCL	GPIO5_IO20	1V8	I/O	General Purpose Input Output
E1_45	E10	I2C3_SCL	I2C3_SCL	1V8	O	I2C bus clock line
E1_46	B7	ECSPI1_MOSI	UART3_TXD	1V8	O	Universal Asynchronous Receive Transmit transmit data signal
E1_47	F10	I2C3_SDA	I2C3_SDA	1V8	I/O	I2C bus data line
E1_48	E13	I2C4_SDA	GPIO5_IO21	1V8	I/O	General Purpose Input Output
E1_49			NC			Not Connected
E1_50	AF7	SAI3_RXD	SAI3_RXD	1V8	I	Integrated Interchip Sound (I2S) channel receive data line
E1_51	AG11	GPIO1_IO06	GPIO1_IO06	1V8	O	Serial Peripheral Interface Chip Select 1 signal
E1_52	AG6	SAI3_TXC	SAI3_TXC	1V8	O	Integrated Interchip Sound (I2S) channel word clock signal
E1_53	A6	ECSPI2_SS0	ECSPI2_SS0	1V8	O	Serial Peripheral Interface Chip Select 0 Signal
E1_54	AC6	SAI3_TXFS	SAI3_TXFS	1V8	O	Integrated Interchip Sound (I2S) channel frame synchronization signal
E1_55	E6	ECSPI2_SCLK	ECSPI2_SCLK	1V8	O	Serial Peripheral Interface clock signal
E1_56	AF6	SAI3_TXD	SAI3_TXD	1V8	O	Integrated Interchip Sound (I2S) channel transmit data line
E1_57	B8	ECSPI2_MOSI	ECSPI2_MOSI	1V8	O	Serial Peripheral Interface master output slave input signal.
E1_58	W23	SD2_CLK	USDHC2_CLK	1V8/ 3V3	O	MMC/SDIO Clock
E1_59	A8	ECSPI2_MISO	ECSPI2_MISO	1V8	I/O	Serial Peripheral Interface master input slave output signal
E1_60	AA26	SD2_CD_B	USDHC2_CD_B	1V8/ 3V3	I	SD Card detect input (Active low)
E1_61	D6	ECSPI1_SCLK	UART3_RXD	1V8	I	Universal Asynchronous Receive Transmit receive data signal
E1_62	W24	SD2_CMD	USDHC2_CMD	1V8/ 3V3	I/O	MMC/SDIO Command
E1_63	B6	ECSPI1_SS0	UART3_RTS_B	1V8	O	Universal Asynchronous Receive Transmit request to send signal
E1_64	V24	SD2_DATA2	USDHC2_DATA2	1V8/ 3V3	I/O	MMC/SDIO Data bit 2
E1_65	A7	ECSPI1_MISO	UART3_CTS_B	1V8	O	Universal Asynchronous

						Receive Transmit clear to send signal
E1_66	AB23	SD2_DATA0	USDHC2_DATA0	1V8/ 3V3	IO	MMC/SDIO Data bit 0
E1_67			NC			Not Connected
E1_68	V23	SD2_DATA3	USDHC2_DATA3	1V8/ 3V3	I/O	MMC/SDIO Data bit 3
E1_69			NC			Not Connected
E1_70	AB24	SD2_DATA1	USDHC2_DATA1	1V8/ 3V3	I/O	MMC/SDIO Data bit 1

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
X1_1			GND		P	Ground
X1_2			GND		P	Ground
X1_3			NC			Not Connected
X1_4	F18	UART4_TXD	GPIO5_IO08	3V3	O	General Purpose Input Output for MIPI Camera 2 power down
X1_5			NC			Not Connected
X1_6	AF11	GPIO1_IO07	GPIO1_IO07	3V3	I/O	General Purpose Input Output for MIPI Display Touchscreen Interupt
X1_7			GND		P	Ground
X1_8			NC			Not Connected
X1_9			NC			Not Connected
X1_10			NC			Not Connected
X1_11			NC			Not Connected
X1_12			NC			Not Connected
X1_13			GND		P	Ground
X1_14			NC			Not Connected
X1_15			NC			Not Connected
X1_16			NC			Not Connected
X1_17			NC			Not Connected
X1_18			NC			Not Connected
X1_19			GND		P	Ground
X1_20			NC			Not Connected
X1_21			NC			Not Connected
X1_22			NC			Not Connected
X1_23			NC			Not Connected
X1_24			NC			Not Connected
X1_25			GND		P	Ground
X1_26			NC			Not Connected
X1_27			NC			Not Connected
X1_28			NC			Not Connected
X1_29			NC			Not Connected
X1_30			NC			Not Connected
X1_31			GND		P	Ground
X1_32			NC			Not Connected
X1_33	AC27	ENET_MDC	ENET_MDC	2V5	O	Management data clock reference
X1_34			NC			Not Connected
X1_35	AB27	NET_MDIO	ENET_MDIO	2V5	I/O	Management data
X1_36			NC			Not Connected
X1_37	R23	SD1_RESET_B	GPIO2_IO10	3V3	O	Ethernet reset

X1_38			NC			Not Connected
X1_39	R24	SD1_STROBE	GPIO2_IO11	3V3	I	Ethernet interrupt output
X1_40			NC			Not Connected
X1_41	AG14	GPIO1_IO00	CCM_ENET_PHY _REF_CLK_ROOT	3V3	O	Synchronous Ethernet recovered clock
X1_42			NC			Not Connected
X1_43	AF24	ENET_TX_CTL	ENET1_RGMII _TX_CTL	2V5	O	RGMII transmit enable
X1_44			NC			Not Connected
X1_45	AF27	ENET_RX_CTL	ENET1_RGMII _RX_CTL	2V5	I	RGMII receive data valid
X1_46			NC			Not Connected
X1_47			GND		P	Ground
X1_48			NC			Not Connected
X1_49	AG24	ENET_TXC	ENET1_RGMII _TXC	2V5	O	RGMII transmit clock
X1_50			NC			Not Connected
X1_51	AG26	ENET_TD0	ENET1_RGMII _TD0	2V5	O	RGMII transmit data 0
X1_52			NC			Not Connected
X1_53	AF26	ENET_TD1	ENET1_RGMII _TD1	2V5	O	RGMII transmit data 1
X1_54			NC			Not Connected
X1_55	AG25	ENET_TD2	ENET1_RGMII _TD2	2V5	O	RGMII transmit data 2
X1_56			NC			Not Connected
X1_57	AF25	ENET_TD0	ENET1_RGMII _TD3	2V5	O	RGMII transmit data 3
X1_58			NC			Not Connected
X1_59			GND		P	Ground
X1_60			NC			Not Connected
X1_61	AE26	ENET_RXC	ENET1_RGMII _RXC	2V5	I	RGMII receive clock
X1_62			NC			Not Connected
X1_63	AE27	ENET_RD0	ENET1_RGMII _RD0	2V5	I	RGMII receive data 0
X1_64			NC			Not Connected
X1_65	AD27	ENET_RD1	ENET1_RGMII _RD1	2V5	I	RGMII receive data 1
X1_66	AF14	GPIO1_IO01	PWM1_OUT	3V3	I/O	General Purpose Input Output with PWM control for MIPI DSI Brightness Control
X1_67	AD26	ENET_RD2	ENET1_RGMII _RD2	2V5	I	RGMII receive data 2
X1_68	AD10	GPIO1_IO10	GPIO1_IO10	3V3	I/O	General Purpose Input Output to enable MIPI DSI Display
X1_69	AC26	ENET_RD3	ENET1_RGMII _RD3	2V5	I	RGMII receive data 3
X1_70			GND		P	Ground

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
X2_1			GND		P	Ground
X2_2			GND		P	Ground
X2_3	AG18	SAI1_RXD4	BT_CFG4	3V3	I	Boot Select pin
	AG21	SAI1_TXD2	BT_CFG10	3V3	I	Boot Select pin
	AG22	SAI1_TXD4	BT_CFG12	3V3	I	Boot Select pin
X2_4	A12	MIPI_DSI_D2_N	MIPI_DSI_D2_N	1V8	O	MIPI Display Serial Interface data pair 2 negative signal
X2_5	G26	BOOT_MODE0	BOOT_MODE0	3V3	I	Boot Select pin
X2_6	B12	MIPI_DSI_D2_P	MIPI_DSI_D2_P	1V8	O	MIPI Display Serial Interface data pair 2 positive signal
X2_7	AF22	SAI1_TXD5	BT_CFG13	3V3	I	Boot Select pin
	AF21	SAI1_TXD3	BT_CFG11	3V3	I	Boot Select pin
X2_8			GND		P	Ground
X2_9	G27	BOOT_MODE1	BOOT_MODE1	3V3	I	Boot Mode1 select
X2_10	A13	MIPI_DSI_D3_N	MIPI_DSI_D3_N	1V8	O	MIPI Display Serial Interface data pair 3 negative signal
X2_11			GND		P	Ground
X2_12	B13	MIPI_DSI_D3_P	MIPI_DSI_D3_P	1V8	O	MIPI Display Serial Interface data pair 3 positive signal
X2_13			NC			Not Connected
X2_14			GND		P	Ground
X2_15			NC			Not Connected
X2_16			NC			Not Connected
X2_17			GND		P	Ground
X2_18			NC			Not Connected
X2_19	AC22	SAI2_TXD0	SAI2_TXD	3V3	O	Integrated Interchip Sound (I2S) channel transmit data line
X2_20			GND		P	Ground
X2_21	AC24	SAI2_RXD0	SAI2_RXD	3V3	I	Integrated Interchip Sound (I^2S) channel receive data line
X2_22			NC			Not Connected
X2_23			GND		P	Ground
X2_24			NC			Not Connected
X2_25	AD23	SAI2_TXFS	SAI2_TXFS	3V3	O	Integrated Interchip Sound (I^2S) channel frame synchronization signal
X2_26			GND		P	Ground
X2_27	AD22	SAI2_TXC	SAI2_TXC	3V3	O	Integrated Interchip Sound (I^2S) channel word clock signal
X2_28			NC			Not Connected
X2_29			GND		P	Ground
X2_30			NC			Not Connected
X2_31	A16	MIPI_CSI_CLK_N	MIPI_CSI_CLK_N	1V8	O	MIPI Camera Serial Interface clock pair negative signal
X2_32			GND		P	Ground

X2_33	B16	MIPI_CSI_CLK_P	MIPI_CSI_CLK_P	1V8	O	MIPI Camera Serial Interface clock pair positive signal
X2_34			NC			Not Connected
X2_35	A14	MIPI_CSI_D0_N	MIPI_CSI_D0_N	1V8	I	MIPI Camera Serial Interface data pair 0 negative signal
X2_36			NC			Not Connected
X2_37	B14	MIPI_CSI_D0_P	MIPI_CSI_D0_P	1V8	I	MIPI Camera Serial Interface data pair 0 positive signal
X2_38			GND		P	Ground
X2_39	B15	MIPI_CSI_D1_P	MIPI_CSI_D1_P	1V8	I	MIPI Camera Serial Interface data pair 1 positive signal
X2_40			NC			Not Connected
X2_41	A15	MIPI_CSI_D1_N	MIPI_CSI_D1_N	1V8	I	MIPI Camera Serial Interface data pair 1 negative signal
X2_42			NC			Not Connected
X2_43	B17	MIPI_CSI_D2_P	MIPI_CSI_D2_P	1V8	I	MIPI Camera Serial Interface data pair 2 positive signal
X2_44			GND		P	Ground
X2_45	A17	MIPI_CSI_D2_N	MIPI_CSI_D2_N	1V8	I	MIPI Camera Serial Interface data pair 2 negative signal
X2_46	A23	USB2_DN	USB2_DN	3V3	I/O	Universal Serial Bus differential pair negative signal
X2_47	A18	MIPI_CSI_D3_N	MIPI_CSI_D3_N	1V8	I	MIPI Camera Serial Interface data pair 3 negative signal
X2_48	B23	USB2_DP	USB2_DP	3V3	I/O	Universal Serial Bus differential pair positive signal
X2_49	B18	MIPI_CSI_D3_P	MIPI_CSI_D3_P	1V8	I	MIPI Camera Serial Interface data pair 3 positive signal
X2_50	F23	USB2_VBUS	USB2_VBUS	5V	I	Universal Serial Bus power
X2_51			GND		P	Ground
X2_52	AD19	SAI2_MCLK	GPIO4_IO27	3V3	I	General Purpose Input Output for Active low input, to inform USB overcurrent condition (low = overcurrent detected)
X2_53	B9	MIPI_DSI_D0_P	MIPI_DSI_D0_P	1V8	O	MIPI Display Serial Interface data pair 0 positive signal
X2_54			GND		P	Ground
X2_55	A9	MIPI_DSI_D0_N	MIPI_DSI_D0_N	1V8	O	MIPI Display Serial Interface data pair 0 negative signal
X2_56	B21	PCIE_CLK_P	PCIE_CLK_P	1V8	O	PCI Express clock differential pair positive signal

X2_57	B10	MIPI_DSI_D1_P	MIPI_DSI_D1_P	1V8	O	MIPI Display Serial Interface data pair 1 positive signal
X2_58	A21	PCIE_CLK_N	PCIE_CLK_N	1V8	O	PCI Express clock differential pair negative signal
X2_59	A10	MIPI_DSI_D1_N	MIPI_DSI_D1_N	1V8	O	MIPI Display Serial Interface data pair 1 negative signal
X2_60			GND		P	Ground
X2_61	A11	MIPI_DSI_CLK_N	MIPI_DSI_CLK_N	1V8	O	MIPI Display Serial Interface clock pair negative signal
X2_62	B20	PCIE_TXN_P	PCIE_TXN_P	1V8	O	PCI Express Receive input differential pair positive signal
X2_63	B11	MIPI_DSI_CLK_P	MIPI_DSI_CLK_P	1V8	O	MIPI Display Serial Interface clock pair positive signal
X2_64	A20	PCIE_TXN_N	PCIE_TXN_N	1V8	O	PCI Express Receive input differential pair negative signal
X2_65	AF12	GPIO1_IO05	GPIO1_IO05	3V3	O	General Purpose Input Output for MIPI Camera reset
X2_66			GND		P	Ground
X2_67	F19	UART4_RXD	GPIO5_IO28	3V3	O	General Purpose Input Output for MIPI Camera power down
X2_68	B19	PCIE_RXN_P	PCIE_RXN_P	1V8	I	PCI Express Receive input differential pair positive signal
X2_69	AC9	GPIO1_IO14	CCM_CLKO1	3V3	O	MIPI Camera input clock
X2_70	A19	PCIE_RXN_N	PCIE_RXN_N	1V8	I	PCI Express Receive input differential pair negative signal

5. PICO Compute Module Connector Interfaces

5.1. Ethernet

The PICO-IMX8M-Mini provides a 10/100/1000-Mbit/s MAC ethernet interface which, implements layer 3 network acceleration functions. These functions are designed to accelerate the processing of various common networking protocols, such as IP, TCP, UDP, and ICMP, providing wire speed services to client applications.

The Ethernet interface provides following features.

- Triple speed 10/100/1000 Mbit/s Ethernet MAC compliant with the IEEE802.3-2002 standard.
- The MAC layer provides compatibility with half- or full-duplex 10/100 Mbit/s Ethernet LANs and full-duplex gigabit Ethernet LANs.

For additional details, please refer to the “Ethernet MAC (ENET)” chapter of the “i.MX8M Mini Applications Processor Reference Manual”.

Table 8 - Ethernet Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
X1_33	AC27	ENET_MDC	ENET_MDC	2V5	O	Management data clock reference
X1_35	AB27	NET_MDIO	ENET_MDIO	2V5	I/O	Management data
X1_37	R23	SD1_RESET_B	GPIO2_IO10	3V3	O	Ethernet reset
X1_39	R24	SD1_STROBE	GPIO2_IO11	3V3	I	Ethernet interrupt output
X1_41	AG14	GPIO1_IO00	CCM_ENET_PHY _REF_CLK_ROOT	3V3	O	Synchronous Ethernet recovered clock
X1_43	AF24	ENET_TX_CTL	ENET1_RGMII _TX_CTL	2V5	O	RGMII transmit enable
X1_45	AF27	ENET_RX_CTL	ENET1_RGMII _RX_CTL	2V5	I	RGMII receive data valid
X1_49	AG24	ENET_TXC	ENET1_RGMII _TXC	2V5	O	RGMII transmit clock
X1_51	AG26	ENET_TD0	ENET1_RGMII _TD0	2V5	O	RGMII transmit data 0
X1_53	AF26	ENET_TD1	ENET1_RGMII _TD1	2V5	O	RGMII transmit data 1
X1_55	AG25	ENET_TD2	ENET1_RGMII _TD2	2V5	O	RGMII transmit data 2
X1_57	AF25	ENET_TD0	ENET1_RGMII _TD3	2V5	O	RGMII transmit data 3
X1_61	AE26	ENET_RXC	ENET1_RGMII _RXC	2V5	I	RGMII receive clock
X1_63	AE27	ENET_RD0	ENET1_RGMII _RD0	2V5	I	RGMII receive data 0
X1_65	AD27	ENET_RD1	ENET1_RGMII _RD1	2V5	I	RGMII receive data 1
X1_67	AD26	ENET_RD2	ENET1_RGMII _RD2	2V5	I	RGMII receive data 2
X1_69	AC26	ENET_RD3	ENET1_RGMII _RD3	2V5	I	RGMII receive data 3

5.2. MIPI Display

The Mobile Industry Processor Interface (MIPI) Display Serial Interface (DSI) controller is a flexible, high-performance, and easy-to-use digital core that implements all protocol functions defined in the MIPI DSI Specification. The MIPI DSI controller provides an interface that allows communication with MIPI DSI-compliant peripherals. The MIPI DSI D-PHY is a high frequency, low power, low-cost, source-synchronous, physical layer supporting the MIPI Alliance standard for D-PHY.

Key features of the MIPI DSI Controller Core include:

- Implements all three DSI Layers (Pixel to Byte packing, Low Level Protocol, Lane Management)
- Support for Command and Video Modes
- Host Version
- Scalable data lane support, 1 to 4 Data Lanes
- Optional bidirectional support on lane 0
- Supports High Speed and Low Power operation
- Support for all DSI data types and formats
- Virtual Channel support
- Supports ULPS mode
- Full Low-Level Protocol Error and Contention detection and reporting
- Supports continuous and non-continuous Clock Lane operation
- Supports multiple packets per transmission
- Support for all three Video Mode packet sequences
    - Non-Burst Mode with Sync Pulses
    - Non-Burst Mode with Sync Events
    - Burst mode
- Support for bus turnaround signaling
- Flexible packet based user interface
- APB interface option (status and control)
- Display Pixel Interface Core (DPI-2) option
- Display Bus Interface Core (DBI-2) option
- Supports PHY Protocol Interface (PPI) compatible MIPI D-PHYs
- MIPI Alliance Specification for Display Serial Interface Version 1.1 compliant

For additional details, please refer to the “MIPI DSI Host Controller (MIPI_DSI)” chapter of the “i.MX8M Mini Applications Processor Reference Manual”.

Table 9 - MIPI Display Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
X2_4	A12	MIPI_DSI_D2_N	MIPI_DSI_D2_N	1V8	O	MIPI Display Serial Interface data pair 2 negative signal
X2_6	B12	MIPI_DSI_D2_P	MIPI_DSI_D2_P	1V8	O	MIPI Display Serial Interface data pair 2 positive signal
X2_10	A13	MIPI_DSI_D3_N	MIPI_DSI_D3_N	1V8	O	MIPI Display Serial Interface data pair 3 negative signal
X2_12	B13	MIPI_DSI_D3_P	MIPI_DSI_D3_P	1V8	O	MIPI Display Serial Interface data pair 3 positive signal
X2_53	B9	MIPI_DSI_D0_P	MIPI_DSI_D0_P	1V8	O	MIPI Display Serial Interface data pair 0 positive signal
X2_55	A9	MIPI_DSI_D0_N	MIPI_DSI_D0_N	1V8	O	MIPI Display Serial Interface data pair 0 negative signal
X2_57	B10	MIPI_DSI_D1_P	MIPI_DSI_D1_P	1V8	O	MIPI Display Serial Interface data pair 1 positive signal
X2_59	A10	MIPI_DSI_D1_N	MIPI_DSI_D1_N	1V8	O	MIPI Display Serial Interface data pair 1 negative signal
X2_61	A11	MIPI_DSI_CLK_N	MIPI_DSI_CLK_N	1V8	O	MIPI Display Serial Interface clock pair negative signal
X2_63	B11	MIPI_DSI_CLK_P	MIPI_DSI_CLK_P	1V8	O	MIPI Display Serial Interface clock pair positive signal
X1_6	AF11	GPIO1_IO07	GPIO1_IO07	3V3	I/O	General Purpose Input Output for MIPI Display Touchscreen Interupt
X1_66	AF14	GPIO1_IO01	PWM1_OUT	3V3	I/O	General Purpose Input Output with PWM control for MIPI DSI Brightness Control
X1_68	AD10	GPIO1_IO10	GPIO1_IO10	3V3	I/O	General Purpose Input Output to enable MIPI DSI Display

5.3. MIPI Camera

This section introduces the MIPI CSI-2 RX subsystem with the CSI-2 RX PHY and host controller. This subsystem handles the sensor/image input and process for all the input imaging devices.

The MIPI-CSI2 Controller has the following key features:

- Implements all three CSI-2 MIPI layers (Pixel to byte packing, low level protocol,
- Lane management)
- Supports unidirectional Master operation
- Transmitter and receiver versions
- Scalable data lane support, 1 to 4 Data Lanes
- Supports high speed mode(80Mbps - 1.5Gbps) per lane, providing 4K@30fps capability for the 4 lanes
- Supports 10Mbps data rate in low power mode
- Includes high speed deserializers
- Loopback testability support
- Support for all CSI-2 data types
- Virtual Channel support
- Support for DPHY Ultra Low Power State (ULPS)
- Error collection support (Rx Only)
- Flexible pixel-based user interface
- Supports user generated packets
- Supports single, double, or quad pixel interface
- Supports PHY Protocol Interface (PPI) compatible MIPI D-PHYs
- Delivered fully integrate and verified with target MIPI D-PHY
- RX Video Interface
- APB Control and Status Register (CSR) interface with IRQ support

For additional details, please refer to the “MIPI CSI Host Controller (MIPI_CSI)” chapter of the “i.MX8M Mini Applications Processor Reference Manual”.

Table 10 - MIPI Camera Control Signals

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
X2_31	A16	MIPI_CSI_CLK_N	MIPI_CSI_CLK_N	1V8	O	MIPI Camera Serial Interface clock pair negative signal
X2_33	B16	MIPI_CSI_CLK_P	MIPI_CSI_CLK_P	1V8	O	MIPI Camera Serial Interface clock pair positive signal
X2_35	A14	MIPI_CSI_D0_N	MIPI_CSI_D0_N	1V8	I	MIPI Camera Serial Interface data pair 0 negative signal
X2_37	B14	MIPI_CSI_D0_P	MIPI_CSI_D0_P	1V8	I	MIPI Camera Serial Interface data pair 0 positive signal
X2_39	B15	MIPI_CSI_D1_P	MIPI_CSI_D1_P	1V8	I	MIPI Camera Serial Interface data pair 1 positive signal
X2_41	A15	MIPI_CSI_D1_N	MIPI_CSI_D1_N	1V8	I	MIPI Camera Serial Interface data pair 1 negative signal
X2_43	B17	MIPI_CSI_D2_P	MIPI_CSI_D2_P	1V8	I	MIPI Camera Serial Interface data pair 2 positive signal
X2_45	A17	MIPI_CSI_D2_N	MIPI_CSI_D2_N	1V8	I	MIPI Camera Serial Interface data pair 2 negative signal
X2_47	A18	MIPI_CSI_D3_N	MIPI_CSI_D3_N	1V8	I	MIPI Camera Serial Interface data pair 3 negative signal
X2_49	B18	MIPI_CSI_D3_P	MIPI_CSI_D3_P	1V8	I	MIPI Camera Serial Interface data pair 3 positive signal
X2_65	AF12	GPIO1_IO05	GPIO1_IO05	3V3	O	General Purpose Input Output for MIPI Camera reset
X2_67	F19	UART4_RXD	GPIO5_IO28	3V3	O	General Purpose Input Output for MIPI Camera power down
X2_69	AC9	GPIO1_IO14	CCM_CLKO1	3V3	O	MIPI Camera input clock

5.4. Audio Interface

The PICO-IMX8M-Mini provides multiple I²S (or I²S) interfaces that support fullduplex serial interfaces with frame synchronization such as I2S, AC97, TDM, and codec/DSP interfaces.

The I²S Interface supports the following features:

- Transmitter with independent bit clock and frame sync supporting 1 data line
- Receiver with independent bit clock and frame sync supporting 1 data line
- Each data line can support a maximum Frame size of 32 words
- Word size of between 8-bits and 32-bits
- Word size configured separately for first word and remaining words in frame
- Asynchronous 128 × 32-bit FIFO for each transmit and receive data line
- Supports graceful restart after FIFO error
- Supports automatic restart after FIFO error without software intervention
- Supports packing of 8-bit and 16-bit data into each 32-bit FIFO word

For additional details, please refer to the “Synchronous Audio Interface (SAI)” chapter of the “i.MX8M Mini Applications Processor Reference Manual”.

Table 11 - I2S-1 Audio Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
E1_50	AF7	SAI3_RXD	SAI3_RXD	1V8	I	Integrated Interchip Sound (I2S) channel receive data line
E1_52	AG6	SAI3_TXC	SAI3_TXC	1V8	O	Integrated Interchip Sound (I2S) channel word clock signal
E1_54	AC6	SAI3_TXFS	SAI3_TXFS	1V8	O	Integrated Interchip Sound (I2S) channel frame synchronization signal
E1_56	AF6	SAI3_TXD	SAI3_TXD	1V8	O	Integrated Interchip Sound (I2S) channel transmit data line

Table 12 - I2S-2 Audio Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
X2_19	AC22	SAI2_TXD0	SAI2_TXD	3V3	O	Integrated Interchip Sound (I2S) channel transmit data line
X2_21	AC24	SAI2_RXD0	SAI2_RXD	3V3	I	Integrated Interchip Sound (I²S) channel receive data line
X2_25	AD23	SAI2_TXFS	SAI2_TXFS	3V3	O	Integrated Interchip Sound (I²S) channel frame synchronization signal
X2_27	AD22	SAI2_TXC	SAI2_TXC	3V3	O	Integrated Interchip Sound (I²S) channel word clock signal

5.5. PCI Express

This block provides information regarding PCIe PHY and its features. PCIe PHY supports 6.0 Gbps data rate and complies to PCI Express base specification 2.1. The functions that are performed by the transceiver include serializing the 8B/10B encoded data for transmission, de-serializing received code groups, and word alignment.

When transmitting, the transceiver accepts two or four 10-bit 8B/10B encoded transmit characters, latches them and serializes the data onto the PCIE_TX_P/PCIE_TX_N differential outputs at 1.5 / 2.5 / 3.0 / 5.0 / 6.0 Gbps. It also performs 8B/10B encoding for 8-bit data from the PIPE interface.

When receiving, the transceiver also samples received serial data on the PCIE_RX_P / PCIE_RX_N differential inputs, deserializes it into two or four 10-bit received characters and detects the K28.5 character (0011111010 or 1100000101) for word alignment. It also applies 8B/10B decoding for 8-bit data to the PIPE interface. PCIe PHY core contains on-chip PLL circuitry for synthesis of the baud-rate transmitting clocks, and extraction of the retimed clocks from the received serial stream.

The following list the key features of the PCIe PHY:

- 1.5 / 2.5 / 3.0 / 5.0 / 6.0 Gbps Serializer / Deserializer
- Compliant with PCI Express Base Specification 2.1
- Compliant with PIPE Specification 2.0
- 8 / 16 / 20 / 40-bit CMOS Interface for Transmitter and Receiver
- 25 / 100 MHz Reference Clock
- K28.5 Detection for Word Alignment
- 8B/10B Encoding / Decoding
- Receiver Detection
- Supports Spread Spectrum Clocking in Transmitter and Receiver

For additional details, please refer to the “PCI Express (PCIe)” chapter of the “i.MX8M Mini Applications Processor Reference Manual”.

Table 13 - PCI Express Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
X2_56	B21	PCIE_CLK_P	PCIE_CLK_P	1V8	O	PCI Express clock differential pair positive signal
X2_58	A21	PCIE_CLK_N	PCIE_CLK_N	1V8	O	PCI Express clock differential pair negative signal
X2_62	B20	PCIE_TXN_P	PCIE_TXN_P	1V8	O	PCI Express Receive input differential pair positive signal
X2_64	A20	PCIE_TXN_N	PCIE_TXN_N	1V8	O	PCI Express Receive input differential pair negative signal
X2_68	B19	PCIE_RXN_P	PCIE_RXN_P	1V8	I	PCI Express Receive input differential pair positive signal
X2_70	A19	PCIE_RXN_N	PCIE_RXN_N	1V8	I	PCI Express Receive input differential pair negative signal

NOTE: The PCIE_TX pair has decoupling capacitors on the PICO Compute Module valued 100nF

5.6. Universal Serial Bus (USB) Interface

The PICO-IMX8M-Mini incorporates a single USB Host controller and an additional USB Host/OTG controller.

Each of the USB controllers provides the following main features:
USB 2.0 Host/OTG Controller

- High-Speed/Full-Speed/Low-Speed OTG core
- HS/FS/LS UTMI compliant interface
- High Speed, Full Speed and Low Speed operation in Host mode (with UTMI transceiver)
- High Speed, and Full Speed operation in Peripheral mode (with UTMI transceiver)
- Hardware support for OTG signaling, session request protocol, and host negotiation protocol
- Support charger detection

USB 2.0 Host Controller

- High-Speed/Full-Speed/Low-Speed Host-Only core
- HS/FS/LS UTMI compliant interface

For additional details, please refer to the “Universal Serial Bus Controller (USB)” chapter of the “i.MX8M Mini Applications Processor Reference Manual”.

Table 14 - USB Host Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
X2_46	A23	USB2_DN	USB2_DN	3V3	I/O	Universal Serial Bus differential pair negative signal
X2_48	B23	USB2_DP	USB2_DP	3V3	I/O	Universal Serial Bus differential pair positive signal
X2_50	F23	USB2_VBUS	USB2_VBUS	5V	I	Universal Serial Bus power
X2_51			GND		P	Ground
X2_52	AD19	SAI2_MCLK	GPIO4_IO27	3V3	I	General Purpose Input Output for Active low input, to inform USB overcurrent condition (low = overcurrent detected)

Table 15 - USB OTG Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
E1_3	D22	USB1_ID	USB1_ID	3V3	I	USB OTG ID Pin
E1_16	B22	USB1_DP	USB1_DP	3V3	I/O	Universal Serial Bus differential pair positive signal
E1_18	A22	USB1_DN	USB1_DN	3V3	I/O	Universal Serial Bus differential pair negative signal
E1_19	AG7	SAI3_RXC	GPIO4_IO29	1V8	I	Over current detect input pin to monitor USB power over current
E1_20	F22	USB1_VBUS	USB1_VBUS	5V	I/O	Universal Serial Bus power
E1_21	AF10	GPIO1_IO09	USDHC3_RESET_B	1V8	O	Universal Serial Bus power enable

NOTE: While using USB OTG in USB HOST mode. The USB_ID pin should have a pull-down resistor to GND.

5.7. SDIO/MMC Interface

The PICO-IMX8M-Mini features a MMC / SD / SDIO host interfaces connected to the NXP i.MX8M Mini integrated “Ultra Secured Digital Host Controller” (uSDHC).

The following main features are supported by uSDHC:

- Conforms to the SD Host Controller Standard Specification version 3.0
- Compatible with the MMC System Specification version 4.2/4.3/4.4/4.41/4.5/5.0
- Compatible with the SD Memory Card Specification version 3.0 and supports the Extended Capacity SD Memory Card
- Compatible with the SDIO Card Specification version 3.0
- Designed to work with SD Memory, MiniSD Memory, SDIO, MiniSDIO, SD Combo, MMC, MMC plus, and MMC RS cards
- Card bus clock frequency up to 208 MHz
- Supports 1-bit / 4-bit SD and SDIO modes, 1-bit / 4-bit / 8-bit MMC modes

The MMC/SD/SDIO host controller can support a single MMC / SD / SDIO card or device.

For additional details, please refer to the “Ultra Secured Digital Host Controller (uSDHC)” chapter of the “i.MX8M Mini Applications Processor Reference Manual”.

Table 16 - SDIO Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
E1_29	AG12	GPIO1_IO04	GPIO1_IO04	3V3	O	SD Card voltage select
E1_58	W23	SD2_CLK	USDHC2_CLK	1V8/ 3V3	O	MMC/SDIO Clock
E1_60	AA26	SD2_CD_B	USDHC2_CD_B	1V8/ 3V3	I	SD Card detect input (Active low)
E1_62	W24	SD2_CMD	USDHC2_CMD	1V8/ 3V3	I/O	MMC/SDIO Command
E1_64	V24	SD2_DATA2	USDHC2_DATA2	1V8/ 3V3	I/O	MMC/SDIO Data bit 2
E1_66	AB23	SD2_DATA0	USDHC2_DATA0	1V8/ 3V3	IO	MMC/SDIO Data bit 0
E1_68	V23	SD2_DATA3	USDHC2_DATA3	1V8/ 3V3	I/O	MMC/SDIO Data bit 3
E1_70	AB24	SD2_DATA1	USDHC2_DATA1	1V8/ 3V3	I/O	MMC/SDIO Data bit 1

5.8. Universal Asynchronous Receiver/Transmitter (UART) Interface

The PICO-IMX8M-Mini Universal Asynchronous Receiver/Transmitter (UART) provides serial communication capability with external devices through a level converter.

The UART includes the following features:

- High-speed TIA/EIA-232-F compatible.
- 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none).
- Programmable baud rates up to 4 Mbps.
- 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud.
- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s).
- Hardware flow control support for a request to send and clear to send signals.
- RS-485 driver direction control.
- DCE/DTE capability.
- RX_DATA input and TX_DATA output can be inverted respectively in RS-232/RS-485 mode.
- Various asynchronous wake mechanisms with the capability to wake the processor from STOP mode through an on-chip interrupt.

For additional details, please refer to the “Universal Asynchronous Receiver/Transmitter (UART)” chapter of the “i.MX8M Mini Applications Processor Reference Manual”.

Table 17 - UART Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
E1_22	F15	UART2_RXD	UART2_RXD	1V8	I	Universal Asynchronous Receive Transmit receive data signal
E1_27	E15	UART2_TXD	UART2_TXD	1V8	O	Universal Asynchronous Receive Transmit transmit data signal
E1_46	B7	ECSPI1_MOSI	UART3_TXD	1V8	O	Universal Asynchronous Receive Transmit transmit data signal
E1_61	D6	ECSPI1_SCLK	UART3_RXD	1V8	I	Universal Asynchronous Receive Transmit receive data signal
E1_63	B6	ECSPI1_SS0	UART3_RTS_B	1V8	O	Universal Asynchronous Receive Transmit request to send signal
E1_65	A7	ECSPI1_MISO	UART3_CTS_B	1V8	O	Universal Asynchronous Receive Transmit clear to send signal

NOTE: it is recommended to use the UART1 interface as system debug where possible and use the UART3 signals in applications where one serial port is required.

5.9. Serial Peripheral Interface (SPI)

The PICO-IMX8M-Mini has an onboard SPI interface that can operate in either master or SPI slave mode.

The SPI Interface includes the following features:

- Data rate up to 52 Mbit/s.
- Full-duplex synchronous serial interface.
- Master/Slave configurable.
- Up-to four chip select signals to support multiple peripherals.
- Transfer continuation function allows unlimited length data transfers.
- 32-bit wide by 64-entry FIFO for both transmit and receive data.
- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable.
- Direct Memory Access (DMA) support.

For additional details, please refer to the “Enhanced Configurable SPI (ECSPI)” chapter of the “i.MX8M Mini Applications Processor Reference Manual”.

Table 18 - SPI Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
E1_51	AG11	GPIO1_IO06	GPIO1_IO06	1V8	O	Serial Peripheral Interface Chip Select 1 signal
E1_53	A6	ECSPI2_SS0	ECSPI2_SS0	1V8	O	Serial Peripheral Interface Chip Select 0 Signal
E1_55	E6	ECSPI2_SCLK	ECSPI2_SCLK	1V8	O	Serial Peripheral Interface clock signal
E1_57	B8	ECSPI2_MOSI	ECSPI2_MOSI	1V8	O	Serial Peripheral Interface master output slave input signal.
E1_59	A8	ECSPI2_MISO	ECSPI2_MISO	1V8	I/O	Serial Peripheral Interface master input slave output signal

5.10. I²C Bus

The PICO-IMX8M-Mini incorporates several I²C interfaces. I²C is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange, Minimizing the interconnection between devices. This bus is suitable for applications requiring occasional communications over a short distance between many devices.
The following features are supported:

- Compliance with Philips I2C specification version 2.1
- Multiple-master operation
- Support for standard mode (up to 100K bits/s) and fast mode (up to 400K bits/s)
- Arbitration-lost interrupt with automatic mode switching from master to slave

For additional details, please refer to the "I²C Controller (I²C)" chapter of the "i.MX8M Mini Applications Processor Reference Manual".

Table 19 - I2C Bus Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
E1_41	D10	I2C2_SCL	I2C2_SCL	1V8	O	I2C bus clock line
E1_43	D9	I2C2_SDA	I2C2_SDA	1V8	I/O	I2C bus data line
E1_45	E10	I2C3_SCL	I2C3_SCL	1V8	O	I2C bus clock line
E1_47	F10	I2C3_SDA	I2C3_SDA	1V8	I/O	I2C bus data line

NOTE: All 1V8 I²C bus data and clock lines for all I²C interfaces have 2.2K Ω pull-up resistors present on the PICO-IMX8M module.

5.11. General Purpose Input / Output (GPIO)

The PICO-IMX8M-Mini has 10 dedicated GPIO pins at 1.8V. Many of the other pins used on the PICO Compute Module can be put in GPIO module however doing so might break scalability with other PICO Compute Modules.
The GPIO signals can be configured for the following applications:

- Data input / output
- Interrupt generation

For additional details, please refer to the “General Purpose Input / Output (GPIO)” chapter of the “i.MX8M Mini Applications Processor Reference Manual”.

Table 20 - GPIO Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
E1_24	N24	NAND_CE0_B	GPIO3_IO01	1V8	I/O	General Purpose Input Output
E1_25	N22	NAND_ALE	GPIO3_IO00	1V8	I/O	General Purpose Input Output
E1_26	P26	NAND_READY_B	GPIO3_IO16	1V8	I/O	General Purpose Input Output
E1_28	P23	NAND_DATA00	GPIO3_IO06	1V8	I/O	General Purpose Input Output
E1_29	AG12	GPIO1_IO04	GPIO1_IO04	3V3	O	SD Card voltage select
E1_30	K24	NAND_DATA01	GPIO3_IO07	1V8	I/O	General Purpose Input Output
E1_32	K23	NAND_DATA02	GPIO3_IO08	1V8	I/O	General Purpose Input Output
E1_34	N23	NAND_DATA03	GPIO3_IO09	1V8	I/O	General Purpose Input Output
E1_42	AG8	SAI3_RXFS	GPIO4_IO28	1V8	I/O	General Purpose Input Output
E1_44	D13	I2C4_SCL	GPIO5_IO20	1V8	I/O	General Purpose Input Output
E1_48	E13	I2C4_SDA	GPIO5_IO21	1V8	I/O	General Purpose Input Output

5.12. Pulse Width Modulation (PWM)

The Pulse Width Modulation (PWM) has a 16-bit counter, and is optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4 x 16 data FIFO.

The PICO-IMX8M-Mini has 4 dedicated PWM pins at 1.8V.

The following features characterize the PWM:

- 16-bit up-counter with clock source selection
- 4 x 16 FIFO to Minimize interrupt overhead
- 12-bit pre-scaler for division of clock
- Sound and melody generation
- Active high or active low configured output
- Can be programmed to be active in low-power mode
- Can be programmed to be active in debug mode
- Interrupts at compare and rollover

For additional details, please refer to the “Pulse Width Modulation (PWM)” chapter of the “i.MX8M Mini Applications Processor Reference Manual”.

Table 21 - PWM Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
E1_33	AG9	SPDIF_RX	PWM2_OUT	1V8	O	General Purpose Input Output with PWM control
E1_35	AF8	SPDIF_EXT_CLK	PWM1_OUT	1V8	O	General Purpose Input Output with PWM control
E1_37	AF9	SPDIF_TX	PWM3_OUT	1V8	I/O	General Purpose Input Output with PWM control
E1_39	AD6	SAI3_MCLK	PWM4_OUT	1V8	O	General Purpose Input Output with PWM control

NOTE: When using PWM1_OUT for MIPI DSI Brightness Control on connector X1 PIN 66. You can only use E1_35 in GPIO mode to avoid conflicts.

5.13. Manufacturing and Boot Control

The PICO-IMX8M-Mini has a number of pins to override the default boot media present on the PICO-IMX8M-Mini Compute Module or enable debug serial loader functionality.

Table 22 - Boot Selection Pins

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
X2_3	AG18	SAI1_RXD4	BT_CFG4	3V3	I	Boot Select pin
	AG21	SAI1_TXD2	BT_CFG10	3V3	I	Boot Select pin
	AG22	SAI1_TXD4	BT_CFG12	3V3	I	Boot Select pin
X2_5	G26	BOOT_MODE0	BOOT_MODE0	3V3	I	Boot Select pin
X2_7	AF22	SAI1_TXD5	BT_CFG13	3V3	I	Boot Select pin
	AF21	SAI1_TXD3	BT_CFG11	3V3	I	Boot Select pin
X2_9	G27	BOOT_MODE1	BOOT_MODE1	3V3	I	Boot Mode1 select

5.13.1. eMMC Boot Mode

The PICO-IMX8M-Mini Compute Module automatically boot from the internal eMMC if the all control signals keep floating or if the pins are connected as follow:

Table 25 – eMMC Boot Mode Configuration

PIN	CPU BALL	eMMC Boot Mode
X2_3	AG18	LOW
	AG21	LOW
	AG22	LOW
X2_5	G26	Not Connected
X2_7	AF22	HIGH
	AF21	HIGH
X2_9	G27	Not Connected

5.13.2. Serial Downloader Boot Mode

To boot the PICO-IMX8M-Mini in Serial Download Mode. The boot signals need to be connected as

Table 23 - Serial Downloader Boot Mode Configuration

PIN	CPU BALL	Serial Downloader Mode
X2_3	AG18	Not Connected
	AG21	Not Connected
	AG22	Not Connected
X2_5	G26	HIGH
X2_7	AF22	Not Connected
	AF21	Not Connected
X2_9	G27	LOW

5.13.3. SD Card Boot Mode

To boot the PICO-IMX8M-Mini from a SD card on the baseboard. The boot signals need to be connected as

Table 24 - SD Card Boot Mode Configuration

PIN	CPU BALL	SD Boot Mode
X2_3	AG18	HIGH
	AG21	HIGH
	AG22	HIGH
X2_5	G26	Not Connected
X2_7	AF22	LOW
	AF21	LOW
X2_9	G27	Not Connected

5.14. Input Power Requirements

The PICO-IMX8M-Mini is designed to be driven with a single input power rail.
The power domain pins have to be connected as follow:

- All GND pins have to be connected to the carrier board ground pane.
- All VSYS pins should be connected to the main power source.

Table 25 - Input Power Signals

POWER Rail	Norminal Input	Input Range	Maximum Input Ripple
VSYS (4pin)	5V	+4.2V to +5.25V	+/- 50mV

5.14.1. Power Management Signals

The PICO-IMX8M-Mini has the following set of signals to control the system power states such as the power-on and reset conditions. This enables the system designer to implement a fully ACPI compliant system supporting system states.

Table 26 - Power Management Signals

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
E1_17	A25	ON_OFF	ON_OFF	3V3	I	Power ON button input signal (Recommended to keep floating)
E1_36			RESET IN	1V8	I	Reset power signal

6. Ordering Information

TechNexion provides a complete product portfolio for the PICO-IMX8M-Mini to assist our customers to evaluate, proto-type, integrate and mass produce solutions with our PICO Compute Modules.

6.1. PICO Compute Module Product Ordering Part Numbers

The PICO-IMX8M-Mini is available in a number of standard configurations. Custom tailored versions with other memory configuration, de-population of interfaces or extended and industrial temperature options are available upon request.

Standard part numbers can be easily found on the PICO-IMX8M-Mini product page on the TechNexion corporate homepage.

6.2. Custom Part Number Rule

The PICO-IMX8M-Mini can be ordered in custom tailored configuration to meet special application requirements and conditions according to the following custom part number creation rules.

Custom part numbers carry Minimum order quantities (MOQ). Please connect with your TechNexion distributor or account manager for conditions and availability.

Part number format: **PICO-IMX8MMx-xx-Rxx-Exx-xxxx-xx-xxxx**

Interface	Code	Description
Processor	IMX8MMQ	NXP i.MX8M Mini Quad
Processor Speed	18	1.8Ghz
Memory	R10	1GB LPDDR4
	R20	2GB LPDDR4
	R30	3GB LPDDR4
	R40	4GB LPDDR4
Storage	E16	eMMC 16GB
	EXX	eMMC other capacity
Wi-Fi / Bluetooth	-	-
	9377	Qualcomm QCA9377 802.11a/b/g/n/ac (2.4 + 5GHz) + Bluetooth 5
Temperature Range	-	Commercial Temperature range (0° to +60° C) (Default)
	TE	Extended Temperature range (-20° to +70° C)
	TI	Industrial Temperature range (-40° to +85° C)
Custom ID	XXXX	Custom Part number ID for customized software loader and special component (BOM)

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